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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,847	09/12/2003	Shivraj G. Dharne	SC13027TC	7053

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EXAMINER	
COX, CASSANDRA F	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/660,847	DHARNE ET AL.	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16-20* is/are allowed.

6)☒ Claim(s) *1,6,11,12 and 15* is/are rejected.

7)☒ Claim(s) *2-5,7-10,13 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/6/04, 1/2/04, 9/12/03*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Takahashi et al. (U.S. Patent No. 6,717,434).

In reference to claim 1, Takahashi discloses in Figure 4A-4B an integrated circuit (104) with a bi-directional level shifter (460), the bi-directional level shifter

comprising: a first signal terminal (473) operable as an input and an output, wherein when being operable as an input, the first signal terminal (473) receives a first signal compatible with a first voltage domain (which is seen to be the outside voltage 5V) of the integrated circuit and wherein when being operable as an output, the first signal terminal (473) provides a shifted signal compatible with the first voltage domain of the integrated circuit; a second signal terminal (which is not labeled but is seen to be the terminal coupled to elements 472 and 471) operable as an input and an output, wherein when being operable as an output, the second signal terminal provides a shifted signal compatible with a second voltage domain (which is seen to be the inside voltage 1.8V or 3.3V) of the integrated circuit and wherein when being operable as an input, the second signal terminal receives a second signal compatible with the second voltage domain of the integrated circuit; and level shift circuitry (472) coupled between the first signal terminal (473) and the second signal terminal, the level shift circuitry translating the first signal compatible with the first voltage domain (which is seen as the outside voltage of 5V) to the shifted signal compatible with the second voltage domain (which is seen as the inside voltage of 1.8V or 3.3V) when the first signal terminal is operable as an input, the level shift circuitry (472) translating the second signal compatible with the second voltage domain (which is seen as the inside voltage of 1.8V or 3.3V) to the shifted signal compatible with the first voltage domain (which is seen as the outside voltage of 5V) when the second signal terminal is operable as an input. The same applies to claim 12.

4. Claims 1, 6, 11-12, and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Fukuoka et al. (Publication No. US2004/0052249).

In reference to claim 1, Fukuoka discloses in Figure 11 an integrated circuit with a bi-directional level shifter, the bi-directional level shifter comprising: a first signal terminal (output of IN34/input of IN35) operable as an input and an output, wherein when being operable as an input, the first signal terminal (output of IN34/input of IN35) receives a first signal compatible with a first voltage domain (VccA) of the integrated circuit and wherein when being operable as an output, the first signal terminal (output of IN34/input of IN35) provides a shifted signal compatible with the first voltage domain (VccA) of the integrated circuit; a second signal terminal (output of IN42/input of IN41) operable as an input and an output, wherein when being operable as an output, the second signal terminal (output of IN42/input of IN41) provides a shifted signal compatible with a second voltage domain (VccB) of the integrated circuit and wherein when being operable as an input, the second signal terminal (output of IN42/input of IN41) receives a second signal compatible with the second voltage domain (VccB) of the integrated circuit; and level shift circuitry (LLC) coupled between the first signal terminal (output of IN34/input of IN35) and the second signal terminal (output of IN42/input of IN41), the level shift circuitry (LLC) translating the first signal compatible with the first voltage domain (VccA) to the shifted signal compatible with the second voltage domain (VccB) when the first signal terminal is operable as an input, the level shift circuitry (LLC) translating the second signal compatible with the second voltage domain (VccB) to the shifted signal compatible with the

first voltage domain (VccA) when the second signal terminal is operable as an input. The same applies to claim 12.

In reference to claim 6, Fukuoka discloses in Figure 11 wherein the level shifter has only signal lines that cross a domain boundary between the first voltage domain (VccA) and the second voltage domain (VccB).

In reference to claim 11, Fukuoka discloses in Figure 11 wherein the integrated circuit further comprises: a first circuit (CT1) coupled to the first signal terminal (output of IN34/input of IN35), the first circuit (CT1) including circuitry (IN35) to enable the first circuit (CT1) to receive the shifted signal from the first signal terminal and circuitry (IN34) to enable the first circuit (CT1) to provide the first signal to the first signal terminal; a second circuit (CT2) coupled to the second signal terminal, the second circuit (CT2) including circuitry (IN41) to enable the second circuit to receive the shifted signal from the second signal terminal and circuitry (IN42) to enable the second circuit (CT2) to provide the second signal to the second signal terminal. The same applies to claim 15.

Allowable Subject Matter

5. Claims 16-20 are allowed.

6. Claims 2-5, 7-10, and 13-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: Claims 2-5 and 13-14 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the level

shift circuitry further includes at least one current cut-off transistor (325, 327), wherein responsive to being non-conductive, the at least one current cut-off transistor (325, 327) operates to cut off current flowing in a current path (from node 303 to node 305) between a first voltage domain voltage supply (V_{DD1}) and second voltage domain voltage supply (V_{DD2}) in combination with the rest of the limitations of the base claims and any intervening claims. Claims 7-9 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the level shift circuitry comprises: a current path between the first signal terminal (ST1) and the second signal terminal (ST2), the current path including a first transistor (325) and a second transistor (327), the first transistor (325) being disposed within the first voltage domain and having a first current terminal coupled to the first signal terminal (ST1), a control terminal coupled to a first voltage domain voltage supply (V_{DD1}), and a second current terminal, and the second transistor (327) being disposed within the second voltage domain and having a first current terminal coupled to the second signal terminal (ST2), a control terminal coupled to a second voltage domain voltage supply (V_{DD2}), and a second current terminal coupled to the second current terminal of the first transistor (325) in combination with the rest of the limitations of the base claims and any intervening claims. Claim 10 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the level shift circuitry further comprises: a first transistor (323) located in the first voltage domain and having a first current terminal coupled to a first voltage domain voltage supply and a second current terminal coupled to the

first signal terminal; a second transistor (321) located in the first voltage domain and having a first current terminal coupled the first voltage domain voltage supply, a second current terminal coupled to the control terminal of the first transistor, and a control terminal coupled to the first signal terminal; a third transistor (311) located in the second voltage domain and having a first current terminal coupled to a second voltage domain voltage supply and a second current terminal coupled to the second signal terminal; a fourth transistor (313) located in the second voltage domain and having a first current terminal coupled the second voltage domain voltage supply, a second current terminal coupled to the control terminal of the third transistor, and a control terminal coupled to the second signal terminal in combination with the rest of the limitations of the base claims and any intervening claims.

8. The following is an examiner's statement of reasons for allowance: Claims 16-20 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the level shift circuitry includes means (325, 327) for cutting off current of a current path including the signal line sourced by a second voltage domain supply when the signal line is at a high voltage in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:30 PM and on alternate Fridays from 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC
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August 4, 2004

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